ABSTRACT OF THE DISCLOSURE

A semiconductor memory with a memory core for dynamically holding data in which a data collision at the time of the semiconductor memory making the transition from a standby state to a nonstandby state is prevented. A first buffer circuit inputs an enable signal for controlling a standby state or a nonstandby state. A second buffer circuit outputs a predetermined logic signal or a read/write signal for controlling the reading of data from or the writing of data to the memory core in accordance with the enable signal. A third buffer circuit outputs an inverted signal obtained by inverting the logic signal or the read/write signal in accordance with the enable signal. A control circuit controls the reading or writing of the data by the read/write signal outputted from the second buffer circuit. A data output control circuit controls the inputting of the data from or the outputting of the data to the outside by the inverted signal or the read/write signal outputted from the third buffer circuit.